CLAIMS

1. A computer system comprising:

a plurality of processing devices;

at least one memory resource shared by the plurality of processing devices;

a memory controller, coupled to the plurality of processing devices and to the shared memory resources, to synchronize the access of shared data stored within the data resource by the plurality of processing devices and to override synchronization among the plurality of devices upon notice that a prior synchronization event has occurred or the memory resource is not to be shared by other processing devices.

2. The apparatus according to claim 1 wherein the plurality of processing devices comprise at least one central processing unit.

3. The apparatus according to claim 1 wherein the memory resource is a page frame memory.

4. The apparatus according to claim 1 wherein synchronization occurs after a translation buffer error.

5. The apparatus according to claim 1 wherein the memory control comprises an issue slot for each device to manage the instructions give each of the plurality of processing devices.

6. A method for managing memory synchronization in a computer system having multiple devices sharing memory resources, comprising the steps of:

determining whether a memory element within the memory resource has changed;

determining whether a memory synchronization event has occurred among the multiple devices;

synchronizing the multiple devices if no synchronization event has occurred.

7. The method of claim 6 further comprising the step of:

determining whether the memory resource is to be shared with more than one of the multiple devices;

preventing synchronizing of the memory resource with the multiple devices if the memory resource is not to be shared.

8. The method of claim 6 wherein the memory resource comprises a page frame memory.

9. The method of claim 6 wherein step a comprises:

determining the occurrence of a translation buffer error.

10. The method of claim 6 further comprising the step of:

generating an issue slot for each device to manage instructions given each of the plurality devices and to observe the change of a memory element and the need for a memory synchronization determination.

11. A computer program product implemented on a computer system, the computer program product having computer useable code to manage memory synchronization in the computer system having multiple devices sharing memory resources, comprising:

computer program code to determine whether a memory element within the memory resource has changed;

computer program code to determine whether a memory synchronization event has occurred among the multiple devices;

computer program code to synchronize the multiple devices if no synchronization event has occurred.

12. The computer program product of claim 11 further comprising:

computer program code to determine whether the memory resource is to be shared with more than one of the multiple devices;

computer program code to prevent synchronizing of the memory resource with the multiple devices if the memory resource is not to be shared.

13. The computer program product of 11 wherein the memory resource comprises a page frame memory.

14. The computer program product of claim 11 further comprising computer program code to determine the occurrence of a translation buffer error.

15. The computer program product of claim 11 further comprising computer program code to generate an issue slot for each device to manage instructions given each of the plurality devices and to observe the change of a memory element and the need for a memory synchronization determination.

16. A shared memory apparatus for use in a distributed computer system comprising:

at least one memory resource shared by a plurality of processing devices within the distributed computer system; and

a memory controller, coupled to the plurality of processing devices and to the shared memory resources, to synchronize the access of shared data stored within the data resource by the plurality of processing devices and to override synchronization among the plurality of devices upon notice that a prior synchronization event has occurred or the memory resource is not to be shared by other processing devices.

17. The apparatus according to claim 16 wherein the plurality of processing devices comprise at least one central processing unit.

18. The apparatus according to claim 16 wherein the memory resource is a page frame memory.

19. The apparatus according to claim 16 wherein synchronization occurs after a translation buffer error.

20. The apparatus according to claim 16 wherein the memory control comprises an issue slot for each device to manage the instructions give each of the plurality of processing devices.

21. A computer system comprising:

a plurality of processing devices;

a system bus coupling each of the plurality of processing devices one with another;

a video system, coupled to at least one of the plurality of processing devices;

at least one memory resource coupled to the system bus and shared by the plurality of processing devices;

a memory controller, coupled to the plurality of processing devices and to the shared memory resources, to synchronize the access of shared data stored within the data resource by the plurality of processing devices and to override synchronization among the plurality of devices upon notice that a prior synchronization event has occurred or the memory resource is not to be shared by other processing devices.

22. The apparatus according to claim 21 wherein the plurality of processing devices comprise at least one central processing unit.

23. The apparatus according to claim 21 wherein the memory resource is a page frame memory.

24. The apparatus according to claim 21 wherein synchronization occurs after a translation buffer error.

25. The apparatus according to claim 21 wherein the memory control comprises an issue slot for each device to manage the instructions give each of the plurality of processing devices.